REMARKS

Applicant herewith amends paragraph [0006] in the specification to provide a missing patent reference. A minor typographical error has also been corrected in paragraph [0006]. The amendments are quite self-explanatory.

Applicant takes this opportunity to inform the Examiner that the present application is related to U.S. Application Serial No. 10/339, 752 titled "Method and System for Delay Control in Synchronization Circuits", which was filed on January 8, 2003 and assigned to the assignee of the present application.

Claims 1-5 were submitted for examination. The present response amends claims 2 and 4-5. After the present claim amendments, claims 1-5 still remain pending in the application.

I. Section 103 Rejection (claims 1-2)

Claims 1 and 2 were rejected under 35 U.S.C. § 103(a) as being obvious over United States Patent No. 6,445,231 to Baker et al. (hereafter "Baker") in view of U.S. Patent No. 5,808,478 to Andresen (hereafter "Andresen"). Applicant traverses the rejection of claims 1 and 2 in view of the following remarks.

As discussed in paragraph [0006] in the present application, Baker teaches a circuit in which the delay line is comprised of both a coarse loop and a fine loop. The coarse loop is designed to produce an output signal having a phase variation from an input signal within a coarse delay stage while the fine loop is designed to produce an output signal having a phase deviation from the input signal which is substantially smaller than the deviation of the coarse loop. The coarse loop is designed to bring the output signal to a near phase lock condition, or phase delayed condition, while the fine loop is designed to achieve a locked condition. Thus, a dual-loop (coarse and fine loops) all digital PLL or DLL can provide a wide lock range while at the same time still providing a tight lock within reasonable time parameters.

Andresen, on the other hand, is directed to an output buffer with a slew rate that is load independent. The output buffer is controlled such that it can drive a load with different drive levels by changing the transconductance internal thereto. A delay block introduces an amount of delay tracking the overall intrinsic delay associated with the output buffer. The intrinsic delay changes with temperature, voltage, and process variations. A variable delay block selectively introduces a determined amount of delay into the delay path which does not vary with process, voltage, and temperature conditions. After these delay blocks, a window comparator compares the actual output voltage level with the desired voltage level to determine the difference therebetween. A control system generates the drive control signal at a value to vary the drive level of the output buffer to reduce the difference between the actual and desired voltage levels.

In rejecting independent claim 1, the Examiner acknowledges Baker's failure to teach a "chain of delay circuits wherein the first is independent of PVT variation and the second is dependent on PVT variation." (Office Action, page 3, item 4.) However, the Examiner relies on Andresen to supply this missing limitation. Assuming, *arguendo*, that the teachings of Baker and the teachings of Andresen can properly be combined, that combination fails to teach or suggest all limitations recited in the independent claim 1. For example, as per the Examiner's observation, even if the variable delay 40 and the intrinsic delay 38 in Andresen's buffer 10 (Andresen, Figs. 1-2) are considered the "first portion" and the "second portion", respectively, of the "delay line" element recited in claim 1, there is still no teaching or suggestion in Andresen of "a control circuit for controlling the delay of said delay line [which includes the first and the second portions]" as recited in claim 1. Nor does Baker teach or suggest such "control circuit" in combination with the "phase detector," the "feedback path," and other elements recited in claim 1. The so-called "delay line" of Andresen (which, according to the Examiner, includes the units 38 and 40 in Fig. 2 in Andresen) is in fact used to generate control signals for the output buffer 14 in Andresen and is not itself controlled by "a control circuit" as required under claim 1. The discussion at columns 3 and 4 in Andresen supports this observation.

Further, even though the Examiner finds Andresen combinable with Baker to reject claim 1, Applicant respectfully disagrees with that finding. Applicant observes that the Examiner

doesn't point to any portion in Andresen where the desirability of combining the teachings of Andresen (e.g., output buffer 10 (Andresen, Figure 1)) with the teachings of Baker (e.g., a delay locked loop design) is taught or suggested.

Based on the foregoing discussion, Applicant asserts that the combined teachings of Baker and Andresen fail to teach or suggest all claim limitations recited in independent claim 1 and, hence, fail to render claim 1 obvious under 35 U.S.C. § 103(a). Reconsideration and allowance of claim 1 is therefore respectfully requested.

In rejecting independent claim 2, the Examiner acknowledges Baker's failure to teach a "chain of delay with a first portion with smaller and, a second portion with larger intrinsic delay value." (Office Action, page 5, item 5.) However, the Examiner relies on Andresen to supply this missing limitation. Again assuming, *arguendo*, that the combination of Baker and Andresen is proper, that combination still fails to teach or suggest all limitations recited in the independent claim 2. For example, although the unit 38 (Andresen, Figure 2) in Andresen provides an "intrinsic delay", Applicant fails to find in Andresen any discussion of the relative duration of the "intrinsic delay" of the variable delay unit 40 (Figure 2, Andresen) as compared to the intrinsic delay provided by the unit 38. In fact, Applicant fails to find any discussion in Andresen teaching that the variable delay unit 40 also has "intrinsic delay" and, if so, the size of that delay as compared to the intrinsic delay provided by the unit 38. The Examiner's reliance on Figures 5-6 in Andresen as teaching "intrinsic delays" of two sizes—one smaller and one larger as required under claim 2—is misplaced and is not supported by the discussion of Figures 5 and 6 in Andresen at columns 6-8 therein.

The independent claim 2 has been amended herein to more clearly recite the series-connected nature of the first and the second portions in the delay line recited in claim 2.

Further, even though the Examiner finds Andresen combinable with Baker to reject claim 2, Applicant respectfully disagrees with that finding. Applicant observes that the Examiner doesn't point to any portion in Andresen where the desirability of combining the teachings of Andresen (e.g., output buffer 10 (including intrinsic delay unit 38 and variable delay unit 40)

(Andresen, Figures 1-2)) with the teachings of Baker (e.g., a delay locked loop design) is taught or suggested.

From the above, Applicant asserts that Andresen fails to supply the larger-smaller intrinsic delay claim limitation missing from Baker, contrary to what is asserted by the Examiner. Therefore, the combined teachings of Andresen and Baker fail to teach or suggest all the claim limitations recited in the independent claim 2 and, hence, fail to render claim 2 obvious under 35 U.S.C. § 103(a). Reconsideration and allowance of claim 2 is respectfully requested.

Based on the foregoing, Applicant asserts that the Examiner has failed to establish a *prima facie* case of obviousness of claims 1 and 2 as required under MPEP §§ 2142, 2143 (Eighth Edition incorporating Revision No. 1, 2003) because the combination of cited prior art references Baker and Andresen fails to teach or suggest all the claim limitations in each of the claims 1 and 2. In view of the arguments given hereinabove, Applicant requests that the Examiner withdraw the § 103(a) rejections of pending claims 1 and 2.

II. Section 103 Rejection (claims 3-5)

Claims 3-5 were rejected under 35 U.S.C. § 103(a) as being obvious over Baker in view of United States Patent No. 5,923,715 to Ono (hereafter "Ono"). Applicant traverses the rejection of claims 3-5 in light of the following remarks. It is noted here that the independent claims 4 and 5 have been amended herein to more clearly recite the series-connected nature of the first and the second circuit paths in the second locked loop recited in claims 4 and 5.

Ono teaches a digital PLL circuit that has a frequency comparator circuit for comparing the frequencies of an output clock signal and a reference clock signal to generate frequency comparator information. A delay control circuit generates a predetermined digital signal based on the frequency comparator information, and a clock signal generating circuit generates the output clock signal of the PLL circuit. The clock signal generating circuit changes the oscillation frequency of the output clock signal in response to the predetermined digital signal generated by the delay control circuit. The number of connected delay stages in a variable delay circuit (of the clock signal generating circuit) is controlled on the basis of the output of the frequency

comparator circuit. Additionally, variable load capacitance circuits in the variable delay circuit are controlled mainly on the basis of the output of the frequency comparator. In this way, a digital PLL having small jitter and a high accuracy is provided.

In rejecting independent claim 3, the Examiner acknowledges Baker's failure to teach "a delay line...having a first circuit path having a stepwise variable capacitive load, and second circuit path in series with first circuit path and having a plurality of stages each having at least two paths." (Office Action, page 6, item 7.) Similarly, in rejecting independent claim 5, the Examiner states that Baker fails to teach "a delay line...having a first circuit path having a plurality of stages each having a variable amount of drive associated therewith and second circuit path having a plurality of stages each having at least a fast and slow path." (Office Action, page 11, item 9.) However, for each of claims 3 and 5, the Examiner relies on Ono to supply the corresponding missing limitation. Applicant asserts, based on the following, that the combination of Baker and Ono fails to teach or suggest all limitations recited in the independent claims 3 and 5.

The independent claim 3 recites, among other things, " a first circuit path having a stepwise variable capacitive load" and "a second circuit path in series with the first circuit path and having a plurality of stages each having at least two paths." (Emphases added.) Applicant asserts that Ono fails to teach or suggest such series-connected circuit paths. According to the Examiner, the "first circuit path" is via the load capacitance control unit 12 in Ono (Figures 1-2, Ono) and the "second circuit path" is via the delay stage control unit 13 in Ono. Applicant initially observes that except for the Up/Down counter 88 in Figure 4(c) in Ono, no additional constructional details of the control unit 13 are provided in Ono. That is, no "plurality of stages" with each stage "having at least two paths" is shown for the control unit 13 in Ono.

Applicant respectfully submits that the Office has misconstrued the teachings of Ono. More specifically, it is believed that Ono fails to disclose a second circuit path which includes a "plurality of stages each having at least two paths." In Figure 2, Ono discloses a variable delay circuit (16) which includes a plurality of inverter pairs (23, 24). As seen in Figure 3, the inverters

in each inverter pair (23, 24) are serially connected (i.e., each stage has a single path). The output of each inverter pair is connected to an input of a multiplexer (20). Ono states:

> One of the input terminals 0 through 2^{s-1} of the multiplexer 20 is selected based on the value of the delay stage control signals E_{s1} through E_{ss}. Because each input terminal of the multiplexer is connected to the output of one of the 2^s stages of inverters, a selected number of stages of inverters (corresponding to the selected input terminal) are connected to the output of the variable delay circuit to generate a predetermined delay value.

(Column 5, lines 1 – 8.) It is respectfully submitted that regardless of which "one of the input terminals ... of the multiplexer 20 is selected," the resulting "second circuit path" does not include "a plurality of stages" wherein each stage has two paths. For example, referring to Figure 2 in Ono, if input terminal 0 is selected, the circuit path serially runs from the input, through inverters 21 and 22, through the multiplexer 20 and to the output. If input terminal 1 is selected, the circuit path includes the inverter stage 23 and serially runs from the input, through inverters 21 and 22, through inverter pair 23, through the multiplexer 20, and to the output. As a result, the smallest delay increment that can be achieved by Ono's circuit is equal to two gate delays (i.e., each inverter in the inverter pair has one gate delay).

In contrast, claim 3 recites "a second circuit path in series with the first circuit path and having a plurality of stages each having at least two paths." The amended independent claim 5 also recites a similar "second circuit path", except that claim 5 specifically recites that the "second circuit path" therein has "a plurality of stages each having at least a fast and a slow path" (i.e., each stage has at least two paths). As discussed in the specification, page 6, paragraph [0027]:

> The embodiment illustrated in FIG. 4 includes a slow path 65 which is comprised of a first inverter 66, a second inverter 67 and a multiplexer 68. A fast path 70 is similarly comprised of a first inverter 71, a second inverter 72, and a multiplexer 73. By varying the size of the inverter in the slow path 65, a different delay resolution can be achieved.

It is respectfully submitted that the claimed combination can achieve a finer delay adjustment than the prior art.

From the foregoing discussion, it is seen that Ono fails to teach or suggest at least the "second circuit path" limitation recited in claims 3 and 5. Therefore, Applicant asserts that the combined teachings of Baker and Ono fail to teach or suggest all claim limitations recited in independent claims 3 and 5 and, hence, fail to render claims 3 and 5 obvious under 35 U.S.C. § 103(a). Reconsideration and allowance of claims 3 and 5 is therefore respectfully requested.

In rejecting independent claim 4, the Examiner acknowledges Baker's failure to teach "a delay line...having a first circuit path having a stepwise variable capacitive load, and second circuit path in series with first circuit path and having a plurality of stages each having a variable amount of drive associated therewith." (Office Action, page 9, item 8.) However, the Examiner relies on Ono to supply the teachings missing from Baker. Applicant asserts, based on the following, that combination of Baker and Ono fails to teach or suggest all limitations recited in the independent claim 4.

The amended independent claim 4 recites, among other things, " a first circuit path having a stepwise variable capacitive load" and "a second circuit path in series with said first circuit path and having a plurality of stages each having a variable amount of drive associated therewith." From the discussion of Ono given hereinbefore, Applicant asserts that Ono fails to teach or suggest such series-connected circuit paths. Applicant notes the Examiner's failure in the Office Action to clearly point out on page 9, item 8 in the Office Action how Ono teaches or suggests the "second circuit path...having a plurality of stages each having a variable amount of drive associated therewith." In any event, Applicant asserts that Ono fails to teach or suggest that each inverter-multiplexer based "circuit path" in Ono has a "variable amount of drive associated therewith" as required under the amended independent claim 4.

As discussed in the specification, page 7, paragraph [0034]:

> FIG. 7 illustrates another example of how the fine delay may be adjusted by adjusting the amount of drive. The phase detector 80 produces the FAST and SLOW control signals which are input to a selection control block 88. The selection control block 88 produces signals for controlling individual drive stages 90, 91, 92, 93. One of the drive stages, drive stage 91, is illustrated as a pair of parallel connected inverters, and one of the inverters is illustrated in detail in FIG. 7A. Thus, the selection control block 88

determines if one or both paths within drive stages 90, 91, 92, 93 are used.

The Examiner does not point out how, if at all, such "second circuit path" is discussed or taught in Ono. Further, Applicant also fails to find in Ono any discussion, teaching or suggestion of variability of drive for each stage in the "second circuit path."

Based on the foregoing discussion, Applicant asserts that the combined teachings of Baker and Ono fail to teach or suggest all claim limitations recited in independent claim 4 and, hence, fail to render claim 4 obvious under 35 U.S.C. § 103(a). Reconsideration and allowance of claim 4 is therefore respectfully requested.

Based on the foregoing, Applicant asserts that the Examiner has failed to establish a *prima facie* case of obviousness of claims 3-5 as required under MPEP §§ 2142, 2143 (Eighth Edition incorporating Revision No. 1, 2003) because the combination of cited prior art references Baker and Ono fails to teach or suggest all the claim limitations in each of the claims 3-5. In view of the arguments given hereinabove, Applicant requests that the Examiner withdraw the § 103(a) rejections of pending claims 3-5.

CONCLUSION

In the present response, all rejections to the claims in the Office Action of June 28, 2004 are believed to have been addressed. Applicants therefore assert that all pending claims 1-5 are in condition for allowance and a notice by the Office to this effect is respectfully requested. If the Examiner has any questions, comments or suggestions, the undersigned Attorney earnestly requests a telephone conference at the Examiner's convenience.

Respectfully submitted,

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